WHAT IS CLAIMED IS

1. A method, using a physical layout system, for physically laying out a microfluidic circuit comprising a plurality of microfluidic components, said method comprising:

placing a first component of said plurality of microfluidic components, wherein said plurality of microfluidic components comprise multilayered components;

placing a second component of said plurality of microfluidic components; and

connecting said first component to said second component.

2. The method of claim 1 wherein a multilayered component includes a control channel on a control layer and a fluid channel on a fluid layer.

3. The method of claim 1 wherein a multilayered component includes an active component.

4. The method of claim 1 wherein a multilayered component includes depth information.

5. The method of claim 1 wherein said plurality of microfluidic components comprises structures having elastomeric material.

6. The method of claim 1 wherein said connecting includes a design rule check.

7. The method of claim 1 wherein said connecting uses a passive component comprising a channel on a single layer.

8. A method, using a computer system, for physically laying out a microfluidic circuit comprising a plurality of microfluidic components, said method comprising:

selecting a template;

placing a first component of said plurality of microfluidic components on said template, wherein said plurality of microfluidic components each have an associated property;

placing a second component of said plurality of microfluidic components on said template; and

connecting said first component to said second component.

9. The method of claim 8 wherein said associated property has at least one of physical scaling, physical property, layer assignment, and functional definition.

10. The method of claim 9 wherein said physical property includes a physical dimension having depth information.

11. The method of claim 9 wherein said physical property includes an element attribute.

12. The method of claim 8 wherein said first component comprises an elastomeric structure.

13. The method of claim 8 wherein said elastomeric structure is formed by bonding together a plurality of layers of elastomer.

14. The method of claim 8 wherein said elastomeric structure is formed in part by depositing a photoresist layer on top of an elastomeric layer.

15. The method of claim 8 wherein each component of said plurality of components includes a representative symbol.

16. The method of claim 8 wherein said first component comprises a control channel which moves an associated rigid silicon material, and a fluid channel formed from an elastomeric material.

17. The method of claim 8 wherein said first component functions as a NAND gate.

18. The method of claim 8 wherein said plurality of microfluidic components include channels, pumps, valves, chambers, cell sorters, DNA fingerprint macros, multiplexers, bridges, pressure oscillators, and layer interconnects.

19. The method of claim 8 wherein said plurality of microfluidic components comprise a structure made from a material selected from the group consisting of a flexible material, a rigid material, or a mixture of rigid and flexible materials.

20. The method of claim 8 wherein said rigid material is a silicon based material.

21. The method of claim 8 wherein said flexible material is an elastomer based material.

22. The method of claim 8 wherein said first component comprises a first control channel and a first fluid channel, said second component comprises a second control channel and a second fluid channel, and said connecting comprises connecting said first fluid channel to said second fluid channel.

23. The method of claim 22 wherein when said first component is on a first fluid layer and said second component is on a second fluid layer, said first fluid channel being connected to said second fluid channel by a via.

24. The method of claim 22 wherein said first control channel is on a control layer and said first fluid channel is on a fluid layer.

25. The method of claim 24 wherein said control layer is separate from said fluid layer.

26. The method of claim 22 wherein said first fluid channel is connected to said second fluid channel by a third fluid channel and wherein when said first control channel is connected to a third control channel that crosses said third fluid channel, said third control channel uses an interconnect bridge to cross said third fluid channel.

27. The method of claim 26 wherein said third fluid channel is reduced in width at and near where said third control channel crosses said third fluid channel.

28. The method of claim 8 wherein said first component comprises a first control channel and a first fluid channel, said second component comprises a second control channel and a second fluid channel, and said connecting comprises connecting said first control channel to said second control channel.

29. The method of claim 8 wherein said connecting comprises auto-routing.

30. The method of claim 8 wherein said connecting comprises routing.

31. The method of claim 8 wherein said connecting comprises a design rule check.

32. A microfluidic circuit physical layout method, using a computer, comprising:

selecting a template comprising an I/O port;

placing a microfluidic component on said template, wherein said microfluidic component comprises a component control channel and a component fluid channel; and

connecting said component control channel to said I/O port.

33. The method of claim 32 wherein said microfluidic component includes an elastomeric structure.

34. The method of claim 32 wherein said connecting includes using a control channel to connect said component control channel to said I/O port.

35. The method of claim 32 further comprising:

placing another microfluidic component on said template; and

connecting said component fluid channel of said microfluidic component to another component fluid channel of said another microfluidic component.

36. A method for physical layout of a microfluidic system, said microfluidic system comprising a plurality of microfluidic components, said method comprising:

placing a component of said plurality of microfluidic components on a first layer of a plurality of layers, said component comprising a first fluid channel and a first control channel;

placing a second fluid channel on a second layer of said plurality of layers; and

connecting said first fluid channel to said second fluid channel using a via.

37. A method for physical layout of a microfluidic system using a computer aided design tool, said microfluidic system comprising a plurality of microfluidic components, said method comprising:

selecting a template, comprising a plurality of layers;

placing a first symbol representing a first component of said plurality of microfluidic components, said first symbol comprising a first fluid channel symbol and a first control channel symbol, said first control channel symbol on a different layer of said plurality of layers than said first fluid channel symbol;

placing a second symbol representing a second component of said plurality of microfluidic components, said second symbol comprising a second fluid channel symbol; and

connecting said first fluid channel symbol to said second fluid channel symbol.

38. The method of claim 37 wherein said template comprises an I/O port and said first symbol comprises a first control channel symbol, said method further comprising connecting said first control channel symbol to said I/O port.

39. The method of claim 37 wherein said plurality of microfluidic components are selected from the group consisting of logic gates, channels, pumps, valves, oscillators, chambers, and layer interconnects.

40. The method of claim 37 wherein symbols are connected according to preset design rules.

41. The method of claim 37 wherein said plurality of microfluidic components are assigned physical scaling.

42. The method of claim 37 wherein said plurality of microfluidic components are assigned physical properties.

43. The method of claim 37 wherein said first component is an active fluidic component.

44. The method of claim 37 wherein symbols of components of said plurality of microfluidic components are placed automatically based on preset design rule constraints.

45. The method of claim 37 wherein symbols of components of said plurality of microfluidic components are placed interactively.

46. The method of claim 37 wherein symbols of components of said plurality of microfluidic components are placed manually subject to predetermined design rule checks.

47. The method of claim 46 wherein said predetermined design rule checks include one or more of the checks on I/O placement, channel size mismatch, dangling channels, overlapping components and channels, and channel spacing.

48. The method of claim 37 wherein the components are placed based on mechanical properties.

49. The method of claim 37 wherein said first symbol is connected to said second symbol automatically using an auto-routing routine.

50. The method of claim 37 wherein said first symbol is routed to said second symbol interactively.

51. The method of claim 37 wherein said first symbol is connected to said second symbol manually using a computer display.

52. A method for validating a physical layout of a microfluidic circuit design comprising a plurality of microfluidic components, said method comprising:

providing said plurality of microfluidic components on a template to form said physical layout of said microfluidic circuit design;

extracting a netlist information from said physical layout; and

physically simulating said physical layout by using a dynamic simulation model for each component of said plurality of microfluidic components on said template and said netlist information.

53. The method of claim 52 wherein physically simulating said physical layout uses a commercially available computer software with the capability to perform laminar computational fluidic dynamic and coupled physics simulations.

54. The method of claim 52 wherein physically simulating said physical layout comprises at least one of analyzing dynamic volumetric flow rates in the

components, analyzing component volumes, and analyzing volumetric capacitances of interconnecting and routing channels in the physical layout.

55. The method of claim 52 wherein physically simulating said physical layout comprises simulating actuation of dynamic fluid flow in the components using control signals generated by a Boolean based language.

56. The method of claim 52 further comprising modifying the physical layout based on results of the physical simulation.

57. The method of claim 52 further comprising modifying the design based on results of the physical simulation.

58. The method of claim 52 further comprising writing the physical layout to a layout file to be used for manufacturing.

59. The method of claim 58 wherein said layout file is in a format selected from the group consisting of Gerber, Postscript, EPS, DXF, GDS II, and HPGL (Hewlett-Packard Graphics Language).

60. A method for device implementation of a microfluidic circuit comprising a plurality of microfluidic components, said method comprising:

providing said plurality of microfluidic components on a template to form a physical layout of said microfluidic circuit design;

writing said physical layout to a layout file to be used for manufacturing;

selecting a pattern for a die to be repetitively laid out on a wafer, said die comprising said physical layout; and

automatically laying out said pattern on said wafer by using said layout file.

61. The method of claim 60 wherein said layout file is in a format selected from the group consisting of Gerber, Postscript, EPS, DXF, GDS II, and HPGL (Hewlett-Packard Graphics Language).

62. A microfluidic circuit design method comprising:

developing synthesizable computer code for a design;

generating a microfluidic circuit schematic, comprising a plurality of symbols for microfluidic components, using said synthesizable computer code;

functionally simulating said microfluidic circuit schematic;

placing and routing on a template said microfluidic components to form a physical layout;

physically simulating said physical layout using dynamic simulation models of said microfluidic components; and

writing to a layout file said physical layout.

63 The microfluidic circuit design method of claim 62 further comprising laying out a die comprising said design on a wafer by using a mask of said layout file,.

64. The method of claim 62 wherein the microfluidic components are selected from the group consisting of channels, pumps, valves, chambers, oscillators, and layer interconnects.

65. The method of claim 62 wherein the microfluidic components are selected from normalized, custom, pre-defined, and user-defined components.

66. The method of claim 62 wherein the microfluidic components are routed according to preset design rules.

67. The method of claim 62 wherein the microfluidic components are assigned physical properties.

68. The method of claim 62 wherein the microfluidic components are active fluidic components.

69. The method of claim 62 wherein the microfluidic components have associated VHDL-AMS or Verilog-AMS models.

70. A microfluidic circuit design system comprising:

a synthesis module for synthesizing software of a design into a schematic having a plurality of connected symbols of microfluidic components;

a design capture module for displaying said schematic;

a functional analysis module for functionally simulating selected microfluidic components of the schematic;

a physical implementation module for placing and routing said microfluidic components into a physical layout according to said design; and

a physical analysis module for physically simulating the components in the physical layout.

71. The system of claim 70 wherein the modules comprise instructions stored in a computer-readable medium.

72. A system for physically laying out a microfluidic circuit having a plurality of microfluidic components, comprising:

a library module comprising information associated with said plurality of microfluidic components;

a design rule checking module having a plurality of layout rules; and

a physical layout module for placing and routing said plurality of microfluidic components on a template using said information and said plurality of layout rules.

73. The system of claim 72 wherein said physical layout module includes an auto-routing module for connecting said plurality of microfluidic components automatically.

74. The system of claim 72 wherein said design rule checking module is configured to perform at least one of the checks on I/O placement, channel size mismatch, dangling channels, overlapping components and channels, and channel spacing.

75. The method of claim 72 wherein said plurality of microfluidic components include channels, pumps, valves, chambers, and layer interconnects.

76. A computer program product stored in a computer readable medium for physically laying-out a microfluidic circuit comprising a plurality of microfluidic components, said computer program product comprising:

code for selecting a template;

code for placing a first component of said plurality of microfluidic components on said template, wherein said plurality of microfluidic components comprise multilayered components;

code for placing a second component of said plurality of microfluidic components on said template; and

code for connecting said first component to said second component.

77. The computer program product of claim 76 wherein a microfluidic component of said microfluidic components comprises a data structure having channel depth information.

78. A system for analyzing a microfluidic circuit having a plurality of microfluidic components, comprising:

a physical layout comprising said plurality of microfluidic components, after placement and routing on a template;

a model library comprising dynamic simulation models for said plurality of microfluidic components; and

a dynamic microfluidic simulator for simulating said physical layout using said dynamic simulation models.

79. A computer program product stored in a computer readable medium for validating a physical layout of a microfluidic circuit design comprising a plurality of microfluidic components, said computer program product comprising:

code for providing said plurality of microfluidic components on a template to form said physical layout of said microfluidic circuit design;

code for extracting a netlist information from said physical layout; and

using a dynamic simulation model for each component of said plurality of microfluidic components on said template and said netlist information, code for physically simulating said physical layout.

80. A computer program product stored in a computer readable medium for device implementation of a microfluidic circuit comprising a plurality of microfluidic components, said computer program product comprising:

code for providing said plurality of microfluidic components on a template to form a physical layout of said microfluidic circuit design;

code for writing said physical layout to a layout file to be used for manufacturing;

code for selecting a pattern for a die to be repetitively laid out on a wafer, said die comprising said physical layout; and

code for automatically laying out said pattern on said wafer by using said layout file.